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AGING CHARACTERISTIC

PRODUCTS: CERAMIC CAPACITORS
SERIES: NCA, NCD, NCM, NCMA, NMC, NMC-H, NMC-L, NMC-M AND NMC-P

Reference: EIA-521 & EIA-198-1F (Section 1.1.2- see below)

EIA-198-1F DIELECTRIC CLASS	DIELECTRIC	TYPICAL AGING RATE OF CAPACITANCE VALUE
CLASS I	NPO (COG)	< 0.1%
CLASS II	X7R, X5R	1.5% ~ 4% PER DECADE HOUR
CLASS III	Y5V	7% PER DECADE HOUR

- THE AGING PHENOMENON; LOSS OF CAPACITANCE OVER TIME, IS REVERSED (RESULTING IN RECOVERY OF LOST CAPACITANCE VALUE) WHEN THE DIELECTRIC IS HEATED ABOVE IT'S CURIE TEMPERATURE (~+125°C).
- PCB REFLOW SOLDERING ASSEMBLY USING CERAMIC CHIP CAPACITORS (MLCCs) WILL RESULT TO DE-AGE THE DIELECTRIC AND RESET THE AGING PROCESS.
- POST SOLDER ASSEMBLY IN-CIRCUIT TEST (ICT) LIMITS SHOULD BE ADJUSTED TO ACCOUNT FOR DIELECTRIC AGING (SEE TABLE BELOW).

EIA-198-1F DIELECTRIC CLASS	DIELECTRIC	TOLERANCE	SUGGESTED POST- SOLDERING HEAT IN-CIRCUIT TEST (ICT) LIMITS
CLASS 1	NPO (COG)	± 5%	± 5%
CLASS 2	X7R, X5R	± 5%	+13% / -5%
		± 10%	+18% / -10%
CLASS 3	Y5V	+80% / -20%	+120% / -20%
CLASS 3	Z5U	± 20%	+40% / -20%

EIA-198-1-F
EIA STANDARD - Ceramic Dielectric Capacitors
Classes I, II, III and IV – Part I: Characteristics and Requirements

1.1.2 Class II
Class II ceramic dielectrics **exhibit a predictable change with time** and voltage. Compensation for the **aging effect** is made by referencing capacitance limits to a future time deemed to be most useful to the buyer; **1,000 hours** is normally chosen